



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,490	12/04/2003	Zi-Ping Chen	681954-45U1	7535

570 7590 01/14/2008
PANITCH SCHWARZE BELISARIO & NADEL LLP
ONE COMMERCE SQUARE
2005 MARKET STREET, SUITE 2200
PHILADELPHIA, PA 19103

EXAMINER

BAUER, SCOTT ALLEN

ART UNIT	PAPER NUMBER
----------	--------------

2836

MAIL DATE	DELIVERY MODE
-----------	---------------

01/14/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/726,490

Applicant(s)

CHEN ET AL.

Examiner

Scott Bauer

Art Unit

2836

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 November 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 and 16-32 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7 and 16-32 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

1. Claims 1-7 & 23-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US 6,309,940) in view of Lai et al. (US 2002/0089017).

With regard to Claim 1, Lee teaches an integrated circuit comprising: a silicon-controlled rectifier (column 1 lines 20-25); a first transistor (27, 28) of a first type (P-

channel FET) integrally formed with the SCR including a first gate (37); a second transistor (25, 26) of a second type (N-channel FET) integrally formed with the SCR including a second gate (38); and a control circuit (V_{in}) which provides a first and second voltage to the first and second gates (37 & 38).

Lee does not teach that the control circuit provides a first holding voltage to the SCR to keep the SCR from latching-up, and in response to a second voltage applied to the first and second gates providing a second holding voltage to the SCR to keep the SCR in the latch-up state.

Lai et al., in Figures 7 A&B, teaches an SCR device used to protect an I/O pad wherein a control circuit is coupled to first and second gates of N and P type FETs and that by driving the gates, the control circuit provides a first holding voltage to the SCR to keep the SCR from latching-up, and in response to a second voltage applied to the first and second gates providing a second holding voltage to the SCR to keep the SCR in the latch-up state (paragraph 0057).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Lee with Lai et al., by coupling the control circuit (244 & 250) taught by Lai et al., at node A, to the control signal (V_{in}) of Lee, for the purpose of avoiding latch-up while the SCR operates at normal condition, but allows for easy triggering of the device in an ESD event (Lai et al. Paragraph 0021).

The integrated circuit taught in Fig. 1 of Lee, is capable of use for electrostatic discharge protection.

With regard to Claims 2-4, Lee in view of Lai et al. discloses the circuit of Claim 1.

Lai et al. further discloses that the control circuit further comprises an output terminal (A) coupled to first and second gates. Lai et al. further teaches that the control circuit comprises a resistor (244), a capacitor (250) and an output terminal (A) disposed between the resistor and the capacitor, which provides a resistor-capacitor delay circuit.

With regard to Claims 5-7, Lee in view of Lai et al. discloses the circuit of Claim 1. Lee further discloses that the SCR further comprising a p-type substrate (11), an n-well (21) formed in the p-type substrate, a p-type diffused region (28) formed in the n-well, and an n-type diffused region (25) formed outside of the n-well. Lee further teaches that the first transistor further comprises a channel region formed in the n-well and that the second transistor further comprises a channel region formed in the p-type substrate (column 1 lines 40-44, 55-59).

With regard to Claim 23, Lee teaches a method of electrostatic discharge protection comprising: providing a silicon-controlled rectifier (SCR) having a holding voltage; integrally forming a first transistor (27 & 28) of a first type with the SCR including a first gate (37); integrally forming a second transistor (25 & 26) of a second type with the SCR including a second gate (38).

Lee does not teach providing a first signal to the first and second gates to raise the holding voltage of the SCR to keep the SCR from latching up; and providing a

second signal to the first and second gates to lower the holding voltage of the SCR to keep the SCR in the latch-up state.

Lai et al., in Figures 7 A&B, teaches an SCR device used to protect an I/O pad wherein a control circuit is coupled to first and second gates of N and P type FETs and that by driving the gates, the control circuit provides a first holding voltage to the SCR to keep the SCR from latching-up, and in response to a second voltage applied to the first and second gates providing a second holding voltage to the SCR to keep the SCR in the latch-up state (paragraph 0057).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Lee with Lai et al., by coupling the control circuit (244 & 250) taught by Lai et al., at node A, to the control signal (V_{in}) of Lee, for the purpose of avoiding latch-up while the SCR operates at normal condition, but allows for easy triggering of the device in an ESD event (Lai et al. Paragraph 0021).

The integrated circuit taught in Fig. 1 of Lee, is capable of use for electrostatic discharge protection.

With regard to Claims 24 & 25, Lee in view of Lai et al. discloses the method of Claim 23. Lai et al. further discloses that the method further comprises raising the holding voltage of the SCR to above a power supply voltage and lowering the holding voltage of the SCR to below a power supply voltage (Lai et al. Paragraph 0057).

With regard to Claim 26, Lee in view of Lai et al. discloses the circuit of Claim 23.

Lee teaches that the SCR is coupled between different voltage lines. Lee does not teach that the SCR is coupled between a contact pad and a voltage line.

Lai et al. In Fig. 4 further discloses that the SCR is coupled between a contact pad (100) and a voltage line (GND).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to place the SCR between a contact pad and voltage line instead of two different voltage lines for the purpose of protecting an internal circuit from an ESD event originating at a contact pad.

With regard to Claim 27, Lee in view of Lai et al. discloses the circuit of Claim 8. Lee et al. Further teaches that the SCR is coupled between different voltage lines (VDD & VSS).

2. Claims 16-22 & 28-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. In view of Lai et al. as applied to claims 1, 8 & 23 above, and further in view of Tong et al. (US 6,756,834).

With regard to Claims 16 & 28, Lee teaches an integrated circuit and a method comprising: a first voltage line (VDD) of a first voltage level; a second voltage line (VSS) of a second voltage level; a silicon-controlled rectifier(SCR), including a p-type transistor and an n-type transistor integrally formed with the SCR.

Lee et al. does not teach a control circuit providing a first holding voltage through the p-type and n-type transistors to the SCR to keep the SCR from latching-up, and providing a second holding voltage through the p-type and n-type transistors to the SCRs to keep the SCRs in the latch-up state during an ESD event that an ESD pulse appears on the first voltage line or one of the contact pads. Further, Lee does not teach providing a plurality of contact pads or that there is a plurality of SCRs.

Lai et al., in Figures 7 A&B, teaches an SCR device used to protect an I/O pad wherein a control circuit is coupled to first and second gates of N and P type FETs and that by driving the gates, the control circuit provides a first holding voltage to the SCR to keep the SCR from latching-up, and in response to a second voltage applied to the first and second gates providing a second holding voltage to the SCR to keep the SCR in the latch-up state (paragraph 0057).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Lee with Lai et al., by coupling the control circuit (244 & 250) taught by Lai et al., at node A, to the control signal (V_{in}) of Lee, for the purpose of avoiding latch-up while the SCR operates at normal condition, but allows for easy triggering of the device in an ESD event (Lai et al. Paragraph 0021).

The integrated circuit taught in Fig. 1 of Lee, is capable of use for electrostatic discharge protection.

Tong et al., in figure 1, discloses an ESD protection circuit comprising a plurality of pads, first and second voltage sources of first and second voltage levels, and a plurality of ESD protection circuits (10 & 14). Tong et al. further teaches that each ESD

protection device contains a control circuit comprising a capacitor (16) and a resistor (18).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings Lee with Tong et al. by protecting a plurality of I/O pads and voltage lines with the SCR device taught by Lee for the purpose of providing ESD protection to an entire chip assembly instead of just a single voltage source.

With regard to Claim 17 & 29, Lee in view of Lai et al. and further in view of Tong et al. discloses the circuit of Claim 16 and the method of Claim 28. Tong et al. further discloses that an ESD device (14) is coupled between the first and second voltage lines (VCC & VSS) and that the remaining ESDs are each coupled between a corresponding contact pad and the second voltage line.

With regard to Claim 18 & 30, Lee in view of Lai et al. and further in view of Tong et al. discloses the circuit of Claim 17 and the method of Claim 29. Tong et al. further discloses, in Figure 1, that the ESD pulse is discharged from one of the contact pads (VCC PAD 1) via a voltage line (VCC1) to voltage line (VSS 1). This event is depicted by PATH_B in Figure 1.

With regard to Claims 19 & 31 Lee in view of Lai et al. and further in view of Tong et al. discloses the circuit of Claim 17 and the method of Claim 29. Tong et al., in

Figure 1, further discloses that an ESD pulse is discharged from the first voltage (VCC 1) line via the second voltage (20) line to one of the contact pads (VSS PAD 1) via PATH_A.

With regard to Claim 20 & 32, Lee in view of Lai et al. and further in view of Tong et al. discloses the circuit of Claim 17 and the method of Claim 29. Tong et al., in Figure 1, further discloses that an ESD pulse is discharged from one of the contact pads (VCC PAD 1) via the second voltage line (20) to a different contact pad (VSS PAD 1) via PATH_A.

With regard to Claim 21, Lee in view of Lai et al. and further in view of Tong et al. discloses the circuit of Claim 16. Lai et al. further discloses that the control circuit comprises a resistor-capacitor delay circuit.

With regard to Claim 22, Lee in view of Lai et al. and further in view of Tong et al. discloses the circuit of Claim 16. Lai et al. further discloses that the control circuit further comprises an output terminal (A) coupled to a gate of each of the p-type and n-type transistors.

Response to Arguments

Applicant's arguments filed 11/01/2007 have been fully considered but they are not persuasive. Applicant first argues that it is unclear whether the circuit of Lee constitutes an SCR structure, especially a structure designed for ESD event protection. Applicant points out that reference to SCR is mentioned only one time in the specification and that the an SCR is not mentioned in the explanation of Figs. 1 & 2 of Lee which the rejection rely upon. In the background section, Lee mentions that CMOS integrated circuits consist of P and N junctions which make up parasitic NPN and PNP bipolar transistors and that as these devices make up an SCR that can be turned on. Although Lee does not use the phrase Silicon controlled rectifier again an examination of Figs 2 & 3A of Lai shows that the parasitic NPN and PNP transistors of Lee and Identical to the SCR of Lai which is described as an SCR. As requested by applicant, a further explanation of the relationship between a CMOS inverter and a parasitic SCR is provided by the attached document: Catherine, Redmond. "Winning the Battle Against Latch-up in CMOS Analog Switches." Analog Dialogue 35-05(2001): 1-3.

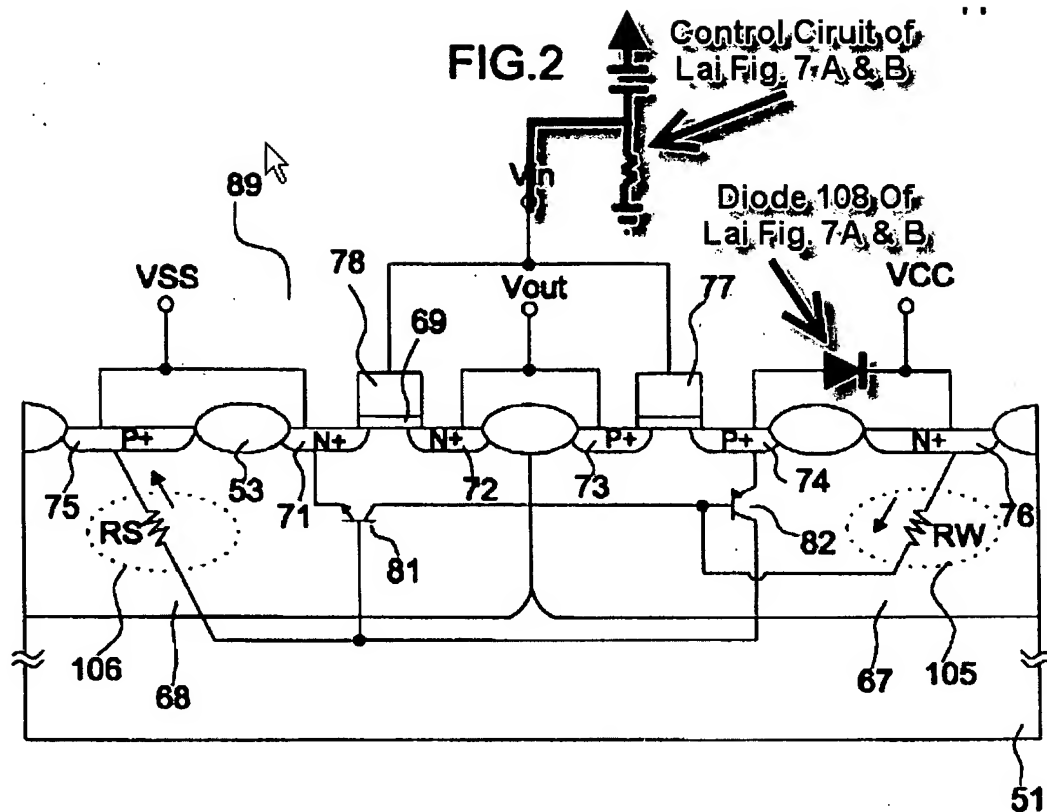
Applicant also argues that Lee does not teach that the SCR is used for ES protection. Firstly, the Lee reference is not relied upon to teach this limitation which is contained in the preamble. Although Lee does not teach that the SCR can be used to shunt an ESD away from an integrated circuit, it is well known in the art that an SCR can be used to protect a load circuit in such a manner. The Lai reference is relied upon to teach such a feature as described in paragraph 0007 of Lai. Further, even if Lai did not teach such a feature, the SCR of Lee is capable of providing such a function as is

know in the art. Further, It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from the prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham*, 2 USPQ2d 1647 (1987). The Lee reference was relied upon for the structure of the circuit and the Lai reference was used to teach how the circuit could be used within a specific application.

Applicant next argues that the Vin of Lee is not a control circuit which provides a first and second voltage to the first and second gates because the circuit of Lee is in reality nothing more than a CMOS inverter and as such, the gates of Lee does not disclose a SCR for ESD protection. However, Even if the device of Lee is a CMOS inverter it still provides a first and second voltage to the first and second gates. Both the circuit of Lai as seen in Fig. 7B and the present invention are CMOS inverters as well. All three inventions comprise a CMOS inverter that has an inherent SCR built into the device. Applicant argues that the voltages of Lee would be low voltage and not the high voltage of an ESD event. Again, this feature is taught by the Lai reference. As in previous responses, Applicant argues that the device of Lee is designed to prevent latch-up during an SCR event and not prevent it at all times except during an ESD event. As described before, the SCR of Lee is resistant to latch up because the resistors 105 and 106 are added to the SCR. This resistors are also present in the Lai reference as it is desirable to only have the SCR trigger when the control signal biases the gates of the circuit. It is desirable for the SCR of Lai to be resistant from latch up as a small transient event that would not trigger the control circuit could inadvertently

trigger the SCR through the well region rather than having it triggered by the lower holding voltage caused by the control circuit. As such, the fact that the device of Lee is Latch-up resistant improves the circuit rather than take away from it. The circuit of Lai differs from the present invention in that the two MOSFETs of the SCR are not formed integrally with the SCR. The Lee reference was used to teach that both MOSFETs could be formed integrally with the SCR. Lastly, Applicant points out that Lee does not teach first and second holding voltages. This Feature is taught by Lai. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Applicant next argues that Lai does not teach that both MOSFETs are integrally formed with the SCR. As mentioned above this feature is taught by Lee. Applicant then argues that the combination of Lee and Lai would require a large amount of modification that would take expensive experimentation and modifications to achieve the configuration claimed by the present invention thus the combination would not have been obvious. However, it is believed that the combination of the two patents would not require a large amount of modification to combine. A study of the schematic of Fig. 7B of Lai shows that slight modification of Lee would cause the device be identical to that described in Fig 7B. If the device of Lee was implemented as shown below, it would provide all of the function claimed in the present invention and be identical to Fig. 7B.



Applicant also argues that a second FET is not provided by Lai and as such, it would be impossible to provide a control circuit attached to first and second integrated FETs. However, as explained above, the control circuit could be connected to two integrated FETs by attaching it to the V_{in} input of Lee as shown above. Applicant then argues that the combination of Lee and Lai would not provide a holding voltage. Lai explains how the circuit of Fig. 7B raises and lowers the holding voltage. In Paragraph 0057, Lai explains that during normal operation the PMOSFET is conducting and the NMOSFET is not conducting. This causes the node connected to the drains of the two MOSFETs of both Lee and Lai to reach VCC . This would bias the collector of the NPN and the gate of the PNP transistors of such that a much larger voltage would be required

to cause latch-up. When the ESD event occurs, Lai explains that the PMOSFET is turned off which causes the voltage at the drains of the two FETs to float which lowers the holding voltage. The NFET then conducts which lowers the triggering voltage and thus shunts the ESD event. This sequence would happen in both the circuits of Lai and Lee if implemented as taught by Lai.

Lastly, applicant argues that it is not clear how the I/O pads or the diode of Lai would be incorporated into the combination of Lee and Lai. This is shown in the figure above. The remaining arguments are similar to those already discussed above and as such have been addressed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Bauer whose telephone number is 571-272-5986. The examiner can normally be reached on M-F 9am-6pm.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 571-272-2084. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Application/Control Number:
10/726,490
Art Unit: 2836

Page 15

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SAB
04 JAN 08

 1-2-08
MICHAEL SHERRY
SUPERVISOR, PATENT EXAMINER
TECHNOLOGY CENTER 2800